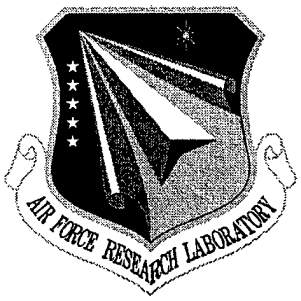
AFRL-SN-RS-TR-1998-222
Final Technical Report
December 1998



SMART PIXELS FOR OPTICAL PROCESSING

Vixel Corporation

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Defense Advanced Research Projects Agency
DARPA Order No. 8680

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AFRL-SN-RS-TR-1998-222 has been reviewed and is approved for publication.

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SMART PIXELS FOR OPTICAL PROCESSING

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Contractor:	Vixel Corporation
Contract Number:	F30602-92-C-0091
Effective Date of Contract:	18 August 1992
Contract Expiration Date:	31 July 1996
Short Title of Work:	Smart Pixels for Optical Processing
Period of Work Covered:	Aug 92 - Jul 96

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This research was supported by the Defense Advanced Research Projects Agency of the Department of Defense and was monitored by James L. Davis, AFRL/SNDP, 26 Electronic Pky, Rome, NY.

REPORT DOCUMENTATION PAGE	Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	Dec 98	Final Aug 92 - Jul 96

4. TITLE AND SUBTITLE

SMART PIXELS FOR OPTICAL PROCESSING

5. FUNDING NUMBERS

C - F30602-92-C-0091
PE - 61101E/62702F
PR - H680
TA - 00
WU - 01

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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

AFRL/SNDP
25 Electronic Pky
Rome NY 13441-4515

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

AFRL-SN-RS-TR-1998-222

11. SUPPLEMENTARY NOTES

AFRL Project Engineer: James Davis, SNDP, 315-330-4276

12a. DISTRIBUTION AVAILABILITY STATEMENT

Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

This work explored the integration of optoelectronic components with traditional electronic GaAs device technologies. The goal was to realize highly functional optoelectronic integrated circuits (OEICs). The intent is to use OEICs to increase performance for demanding military applications such as wideband interconnects, computing, neural networks, pattern recognition, and communications. This program consisted of three phases of work. First Heterojunction Bipolar Transistors (HBTs) were integrated with Vertical-Cavity Surface Emitting Lasers (VCELS). Devices were successfully fabricated and demonstrated. Second, improved HBT/VCSEL devices were designed and fabricated. Third, PIN detector diodes were integrated with VCSELs for application as an optical interconnect element or as an optical processing element (smart pixel). A 2 x 16 VCSEL/PIN array was fabricated and characterized. Recommendations for device improvements and future work are provided.

14. SUBJECT TERMS

Optoelectronic Integrated Circuits (OEICs), Vertical-Cavity Surface Emitting Lasers (VCSELs), Heterojunction Bipolar Transistors (HBTs), Gallium Arsenide, optical interconnects, monolithic integration

15. NUMBER OF PAGES

44

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

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LIST OF ACRONYMS

APC	Automatic Power Control
CML	Current Mode Logic
DBR	Distributed Bragg Reflector
FET	Field Effect Transistor
GaAs	Gallium Arsenide
HBPT	Heterojunction Bipolar Photo-transistor
HBT	Heterojunction Bipolar Transistor
LEOS	Lasers and Electro-Optics Society (IEEE)
LIV plots	Light / Current / Voltage Plots
MBE	Molecular Beam Epitaxy
MESFET	Metal-Semiconductor Field Effect Transistor
OEIC	Optoelectronic Integrated Circuit
PIN diode	P-type / Intrinsic / N-type diode
PL	Photoluminescence
PR	Photoresist
PRI	Photonics Research Incorporated
RIN	Relative Intensity Noise
SCL	Source Coupled Logic
SEM	Scanning Electron Microscope
SI substrate	Semi-Insulating Substrate
VCL	Vertical Cavity Laser
VCSEL	Vertical-Cavity Surface Emitting Laser

ACKNOWLEDGEMENTS

This work was sponsored by the Defense Advanced Research Projects Agency (DARPA) and the U.S. Air Force Rome Laboratory.

1 Introduction and Background

Cielo's predecessor company, Photonics Research Inc., (PRI), submitted the original proposal for this work in January 1992. PRI subsequently reincorporated as Vixel Corporation in 1995. In 1998, the company split into two separate businesses, Cielo Communications, Inc. and Vixel Corporation. Cielo is located in Broomfield, Colorado at the same location where most of this program was performed.

At the time of the proposal, optical semiconductors including semiconductor laser diodes were becoming readily available at reasonable costs. Systems researchers conceived of optoelectronic systems, which exploited optical technology to achieve higher performance than purely electronic systems. For example, optical neural networks were researched as a concept, well before the components needed to build them were available. These conceptual optoelectronic systems were being demonstrated as laboratory prototypes typically by connecting large numbers of individual, discrete optical and electronic components together and adjusting the performance of each component to achieve a working system.

In early 1992 it was clear that a concerted effort to develop techniques of integrating multiple optoelectronic and electronic components could have a substantial payoff. If system builders could use "building blocks" with consistent performance from one component to another, they could come closer to the theoretical performance levels of optoelectronic systems than previously achieved in practice.

PRI was formed in 1991 by a group of accomplished researchers in the field of Vertical-Cavity Surface-Emitting Lasers (VCSELs). They proposed this program to Rome Laboratory and DARPA as an initiative, which would have wide ranging benefits. Much of the conceptual and practical research in optoelectronic systems was being done at U.S. government laboratories, including Rome Laboratory. There were also considerations of promoting the availability of U.S.-based sources for advanced optoelectronic components. PRI intended to develop the processes and techniques to build leading-edge optoelectronic components, including VCSELs, and also to integrate electronic components in order to enable Optoelectronic Integrated Circuits (OEICs).

2 Program Goals

The objective of this effort was to monolithically integrate transistors with semiconductor lasers to form "building blocks" upon which to develop sophisticated Optoelectronic Integrated Circuits (OEICs). The OEICs would be targeted to applications such as: optoelectronic interconnects, digital optical computing, neural networks, pattern/target recognition, laser projection displays, and optical communication.

The scope of the work was to develop optical computing/logic switching approaches that mesh smoothly with the standard electronic computing/logic approaches. This would then be amenable to further development work and could lead to sophisticated and functional OEICs suitable for systems integration.

The proposed "building blocks" would consist of two physical components: (a) an input component (transistor) that is sensitive to electrical or optical input signals and can produce sufficient current to drive the output component and (b) an output component (laser diode) that produces a light-emitting output.

The most important objective was to select the electrical-input/optical-output and optical-input/optical-output devices best suited to be monolithically integrated with standard GaAs bipolar and field-effect technologies.

3 Approach

The approach taken was first to select the devices to be used in the "building blocks", then to optimize the device design and fabrication technologies, and then to fabricate each device and evaluate its performance.

3.1 Device Selection

The first and most important choice was the optical transmitter. Among the possibilities were semiconductor laser diodes (spatial light sources) and spatial-light modulators. At the outset we selected semiconductor laser diodes on the basis that systems based on light sources would have the simplest optical interconnection architecture. Having selected semiconductor laser diodes, the next choice was between edge-emitting and surface-emitting lasers. We selected the Vertical-Cavity Surface-Emitting Laser diode (VCSEL) on the basis that VCSELs could be made one to two orders of magnitude smaller in area than any other surface or edge-emitting diode laser. Also the VCSEL topology facilitates integration of VCSELs with electronic devices and micro-optical components.

The second most important choice was what to use for the electrically/optically sensitive input component of the "building blocks". In 1992 the two clear choices were the GaAs Field-Effect Transistor (FET) and Heterojunction Bipolar Phototransistor (HBPT). These devices had been produced at numerous companies using epitaxial layer structures comparable to those used for laser diodes. Specifically we opted to investigate the following combinations:

- Optically/electrically-controlled HBPT with base contacts, integrated with a VCSEL diode and precursory HBPT development (compatibility with diode laser technology).
- Voltage-controlled FET integrated with a VCSEL diode and precursory FET demonstration (compatibility with diode laser technology).

These bipolar and field-effect transistor/VCSEL combinations were compatible with the dominant GaAs logic circuit topologies, Current-Mode logic (CML) and Source-Coupled Logic (SCL). The bipolar transistors were also sensitive to optical inputs while the field-effect transistors were not.

3.2 Optimize Device Design and Fabrication Technology

The choices were constrained by electronic circuit design and semiconductor growth and processing considerations. A number of different configurations were possible. Among the key choices were:

- Should the VCSEL have a p-contact (mirror) up or n-contact (mirror) up?
- Should the substrate be conducting or insulating?
- How to achieve co-integration of the "building blocks" with dense GaAs digital electronic circuits?
- Should the FETs be n-channel, p-channel, depletion-mode, or enhancement mode?
- What techniques to use to avoid unwanted optical feedback in three-terminal HBPT/VCSEL combinations?
- How to lower and dissipate the ohmic heat generated by the "building blocks"?

- How to address non-planarity issues (low mesas are preferred to high mesas)? How to achieve deep trench isolation in GaAs (as commonly used in Si technology)?

The VCSEL design selected incorporated features of the demonstrated designs reported by Jewell et al. (1990), Lee et al. (1990), and by Yang et al. (1991). The structure consists of an n-type distributed Bragg reflector (mirror, DBR) a quantum-well active region and a dielectric (or p-type) mirror. A key feature to incorporate was the use of the demonstrated dielectric-mirror/p-type-contacting-layer combination, for its lower electrical resistance compared to a p-type mirror. Figure 1 presents an illustration of the VCSEL geometry.

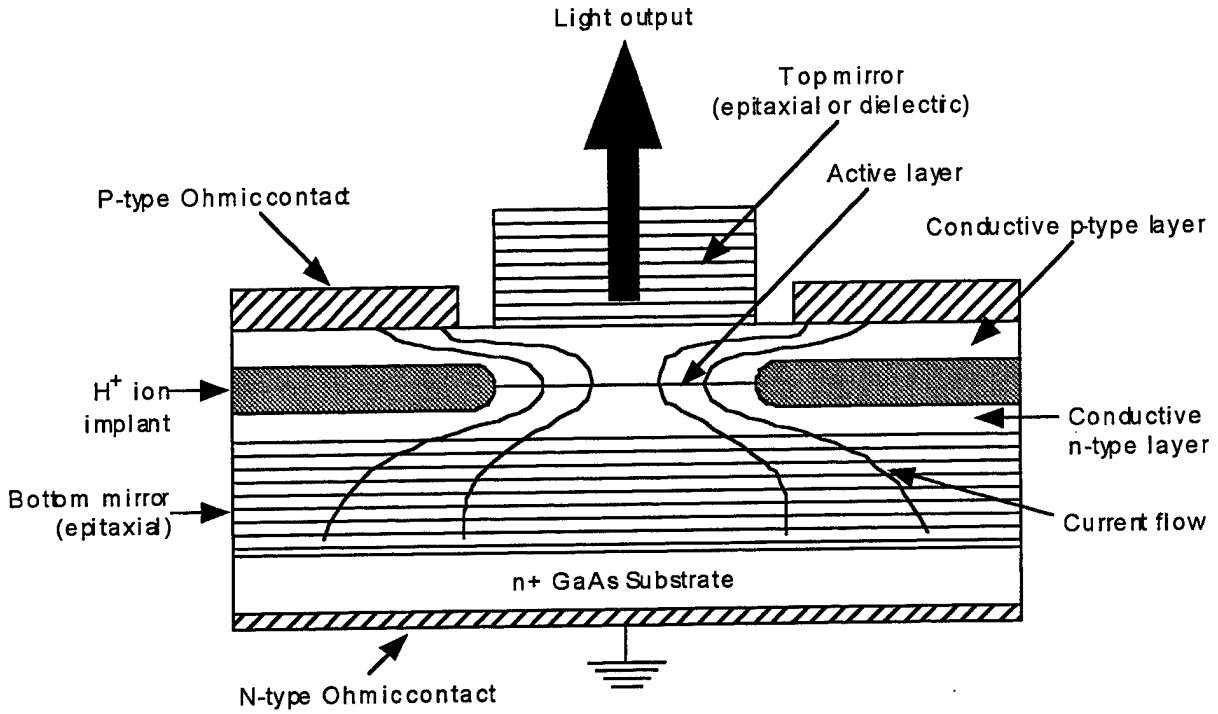


Figure 1 Schematic of a VCSEL geometry for integration with transistors.

The choice of substrate was a difficult one. Complex GaAs electronic circuitry requires fabrication on a semi-insulating substrate in order to provide isolation from one device to another. This contrasts with the VCSEL shown in Figure 1, which is grown on an n-doped GaAs substrate.

If we grew the VCSEL on a SI substrate, in order to make contact between an electrical transistor and the bottom of a VCSEL, either a fourth-level deep trench etch and contact, or a backside via etch to the doped epitaxial layers would be needed. Both approaches would significantly complicate the fabrication. Either approach permits the use of a common n-type layer for the collector of an n-p-n transistor and the cathode of a p-contact-down VCSEL. However since both approaches add significant complexity to the process, and the focus of the research was to be on single device integration, we decided to use a doped substrate to keep the fabrication as simple as possible.

3.3 Selection of "Building Blocks"

3.3.1 Three-Terminal HBPT/VCSEL

The three-terminal HBPT/VCSEL is an integrated transistor-driver/laser with electrical/optical input and optical output. A low-current (10's of μA) or optical signal (10's of μW) is injected or absorbed into the

base and collector regions of the HBPT. This produces current that is internally amplified by the transistor to several mA to drive the VCSEL above threshold. The primary attribute of the HBPT/VCSEL combination is the low current level that is compatible with GaAs electronic integrated circuits. It also benefits from its ability to have or not have optical feedback from the laser latch the device. The close proximity of the transistor driver to the VCSEL minimizes the distance over which high-power signals are transported.

Figure 2 shows a possible three-terminal HBPT/VCSEL structure with the HBPT-up and integrated side-by-side with the VCSEL. This configuration is broadly applicable since it allows top-surface emitting laser operation, which is suited for all wavelengths, e.g., 850 nm or visible. A bottom-emitting VCSEL would have to either operate at a wavelength in the substrate's transparency region, >950 nm, or have the substrate removed. The HBPT-up configuration also allows for processing at very shallow depths, at the elevation of the HBPT.

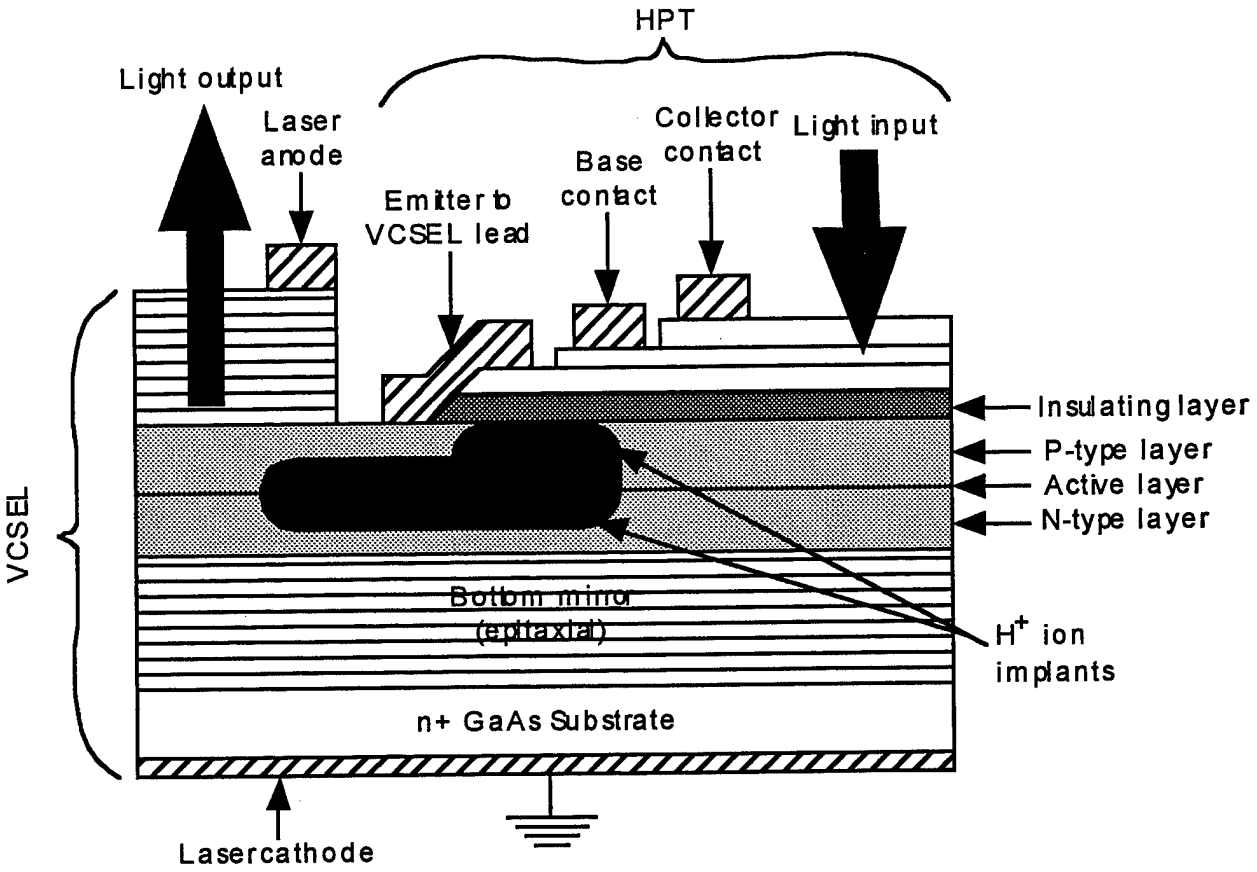


Figure 2 Three-terminal HBPT/VCSEL with the HBPT up and integrated side-by-side with the VCSEL.

3.3.2 Three-Terminal FET/VCSEL

The FET/VCSEL is also an integrated driver/laser, which is complementary to the HBPT/VCSEL. While the HBPT/VCSEL is designed for current control and vertical integration, the FET/VCSEL utilizes voltage control, which integrates quite readily into more complex FET-based circuitry. The device should also be easier to process. The only sensible integration geometry is side-by-side as shown in Figure 3.

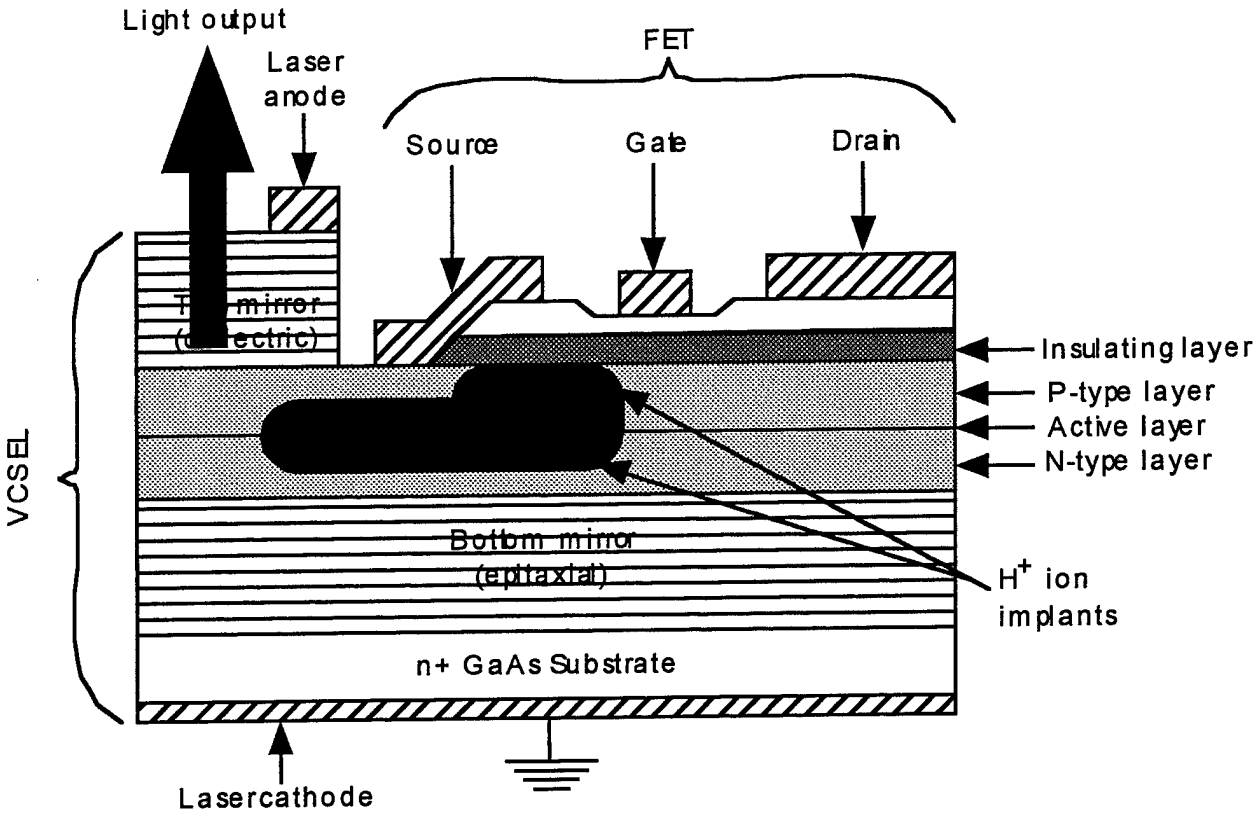


Figure 3 FET/VCSEL device combination.

The combination has a high level of process compatibility with more complex FET-based circuitry. Fabricating other FETs using the same epitaxial layers and the same processing steps as the driver-FET could form complex circuits.

All processing would be at fairly shallow depths, a few microns. As shown in Figure 3, a two-step implant might be required. The deeper implant would isolate the VCSEL cavity, and the shallower implant would isolate the source current from conducting through the stratified p-doped layer while allowing the FET source to contact the VCSEL. Using metal semiconductor technology (MESFET) for the n-channel gate contact avoids high-temperature dopant activation cycles as required for junction FETs.

4 Technical Objectives

The technical objectives that PRI took on were ambitious and if achieved would lead to substantial future work.

4.1 Device Design, Fabrication and Testing

- Design devices and corresponding fabrication processes suitable for future development into highly functional optoelectronic circuits and suitable for eventual integration into systems. Specify the epitaxial structure and processing procedure for each device, and layout photolithographic mask sets. Prior to beginning costly semiconductor growth, processing and device fabrication, conduct a thorough analysis and design of the optical and electronic device properties. Also design a device fabrication sequence optimized for successful device demonstration.

- Fabricate each device and evaluate its performance. Before fabricating the actual proposed devices, perform pre-fabrication, e.g., fabricate FETs on simple epitaxial structures that contain the unique VCSEL features. Device fabrication includes molecular beam epitaxial (MBE) growth, metallization, dielectric mirror deposition, photolithography, ion implantation, reactive ion and/or chemical etching, surface and structural characterization, thermal annealing and electrical and optical characterization. Demonstrate the fabricated devices at PRI's facility.

4.2 Opto-Electronic Integrated Circuit (OEIC) Design

- Design circuits based upon the "building blocks" to perform (a) inverter and (b) Boolean logic functions. Formulate a plan for the development of these OEICs.

- Design optimized monolithically integrated circuits consisting of FETs, HBPTs and VCSELs and perfect designs to perform functions such as: inversion, optical limiting, and boolean logic gates.

- Use the interactive process of design, fabrication, testing, circuit design and the study of system requirements to develop practical optoelectronic circuitry.

4.3 Systems Integration Study

- Study the system requirements of the OEIC circuits for such systems applications as (a) optoelectronic interconnections, (b) optical computing.

- Conduct the systems integration study in conjunction with the OEIC design task. The results of this task provide the basis for future development of OEIC circuits, which in turn are to be incorporated into practical optoelectronic circuits.

- To ensure useful (not simply novel) devices, conduct an extensive study of the specific requirements of systems where optoelectronics can play a significant role. In particular examine the needs of an optoelectronic interconnect system for board-to-board and chip-to-chip communication. The goal is to develop compact, low-power-consumption, wide-bandwidth optical interconnects that can be driven by small "internal-node" sized transistors.

- Study the development of 3D computers with GHz clock speeds and the capability of orders of magnitude increase in computation speed and power.

- Examine the system integration of "building block" components into an addressable laser array system. Such a system would have an enormous range of applications that include: optical

processing (e.g., digital optical computing, pattern recognition, optical neural networks, etc.), input sources to optical computers and correlators, and reading from and writing to optical memory.

- Examine the system area of optical communication and switching. Optical switching logic arrays have the potential to find applications in optical computers, neural networks, pattern recognition, optical correlators, and switching networks. The goal of an optical communication system is to develop a technology for photonic switching applications with an emphasis on large parallel optical information processing.

5 Accomplishments

The previous sections described the objectives as they were at the beginning of the program in August 1992. Inevitably, large multi-year programs reach a point at which it is necessary to revisit the objectives. This program was no exception. There were three major phases of the program.

The first phase focused on HBPT/VCSEL integration – which was successful but took 2 years to complete. HBPT/VCSEL integration was demonstrated but performance was less than ideal. At that time PRI in consultation with Rome Labs redefined the objectives for the final year of the contract.

Phase 2 focused on improving HBT/VCSEL performance and also developing and demonstrating automatic VCSEL power control. Power monitoring of a VCSEL-based device was identified as a major need during phase 1. This phase was also successful but the need for automatic power control was eclipsed by large and rapid improvements in VCSEL device performance.

Another redefinition of objectives occurred leading to a phase 3, which took most of 1996 to complete. Phase 3 was focused on the development of integrated input-PIN diodes and VCSELs. This work, which was also successful, was seen as the optimum direction to go since optical system architectures were rapidly moving in the direction of using commercial technologies.

5.1 Phase 1

The objective of Phase 1 was to demonstrate the monolithic integration of a HBT and a VCSEL.

The first task was to develop an implant mask that could withstand the deep implant required for a VCSEL structure. An electroplated Au on photoresist structure was developed. It consisted of a thick layer of Au, which allowed for high implant energy, sitting atop a photoresist layer, which allowed for easy removal of the Au after implantation. A schematic of the implant mask is shown in Figure 4.

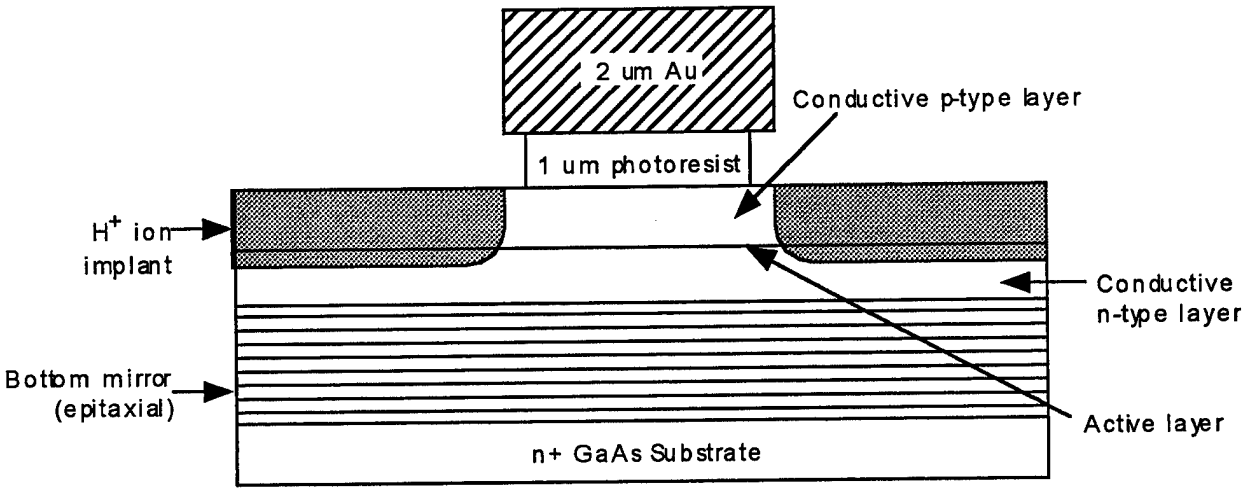


Figure 4 Schematic of Ion Implantation Mask

Next, the resistance of the VCSELs was too high. The likely causes were either 1) contact resistance or 2) a highly resistive p-mirror. The transmission line method was used to measure the contact resistance.

It was found that the contact resistance did not account for the high device resistance. Therefore, it was concluded that the p-mirror was the source of the problem.

The first attempt at rectifying the resistance problem was to increase the p-type doping in the mirror. This modification caused a small, but insufficient, improvement in the overall device resistance. Finally, the problem was traced to the abrupt heterojunction interfaces in the p-mirror layers. The solution was to grade the mirror interfaces. This was achieved in the MBE reactor through fast shutter operations, which produced a digital grade. Upon implementing this solution, the VCSEL voltages and resistances dropped significantly.

The design issue of isolation between HBT and VCSEL was addressed in this phase. Three possible interface layers were considered:

- Low-temperature AlGaAs
- Undoped AlAs
- Undoped GaAs.

In addition to the isolation layers, an appropriate etch stop layer was needed for processing reasons. Low temperature AlGaAs was problematic because of the poor quality of the material grown on top of it. A 0.5 μm non-intentionally doped (NID) GaAs layer with a 25 nm underlying AlAs etch stop layer was used for the initial successful material growths.

Two critical technologies for processing the integrated HBT-VCSEL structure were a HBT mesa definition (and VCSEL exposure) technique and an HBT-VCSEL interconnection technique. The mesa etch developed consisted of a citric acid-based wet chemical etch which preferentially attacked GaAs and low-Al content AlGaAs over AlAs. After the etch reached the etch stop layer, an additional HCl-based etch was used to remove the etch stop layer and expose a smooth VCSEL p-contact layer. The problem of contact between the top of the HBT and the VCSEL p-contact was solved with the use of an air-bridge contact. Similar to the implant mask, Au posts were plated onto the contacts, the surface was planarized with resist and the posts connected via a liftoff metallization step. These techniques represent key technologies for integration of optoelectronic elements.

At this point the HBT-VCSEL design and process were complete. Wafers were grown and fabricated. An Electroglas autoprobe system was used to characterize the devices. Operational HBT-VCSELs were demonstrated. The following is a list of key parameters achieved in phase 1:

- HBT large signal gain 350
- VCSEL threshold voltage 2.7 V
- VCSEL threshold current 19 mA
- HBT base current to reach threshold 48 μA
- HBT base current to reach 1 mW 55 μA
- External Quantum Efficiency 150 W/A
- HBT-VCSEL breakdown voltage 4.5 V

In summary, the first building block of an optoelectronic integrated circuit was successfully developed in the first two years of the contract.

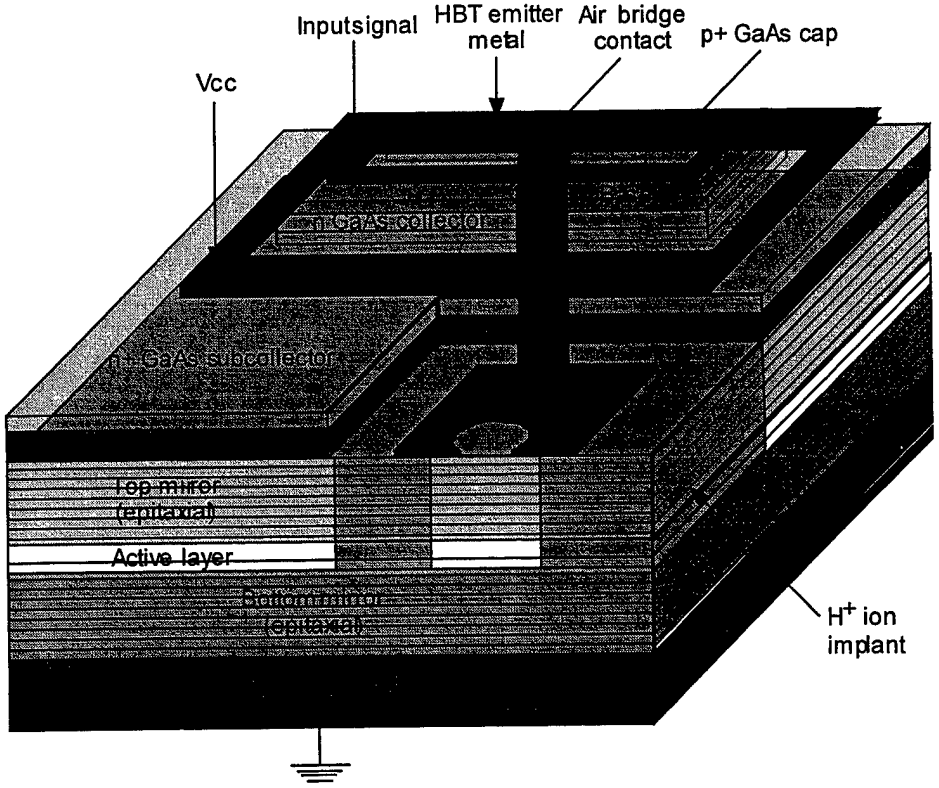
5.2 Phase 2

At the end of Phase 1 the objectives of the contract were reviewed. It was suggested that PRI shift its focus to the following goals:

- Demonstrate an improved HBT-VCSEL.
- Continue to search for applications of this technology.
- Focus on automatic power control (APC) applications and learn their requirements, especially as it relates to laser printing, data communications, and sensor applications.
- Develop automatic power control.
- Demonstrate power monitoring in VCSEL-based device as the enabling technology for APC.

Several improvements in the HBT-VCSEL were made. In particular, the base thickness of the HBT was reduced to allow for larger gain. In addition, the quality of the VCSEL material and processing was carefully monitored to reduce the threshold current. The resulting device parameters showed a significant performance improvement. The VCSEL threshold current was reduced to between 5 and 7 mA, while the threshold voltage increased slightly to 3 to 3.5 V. The maximum power output was raised to 4 to 5 mW. The base current required to drive the VCSEL to threshold was reduced to 43 μA. Finally the power gain was calculated to be 20 mW/mA. These results represent a substantial improvement in the HBT-VCSEL performance. At this point the HBT-VCSEL work was concluded.

Results achieved are illustrated in Figure 5 (structure), Figure 6 (VCSEL performance), Figure 7 (HBT characteristics and VCSEL output), and Figure 8 (HBT base current – VCSEL output).



5. Phase 2 HBT/VCSEL Structure

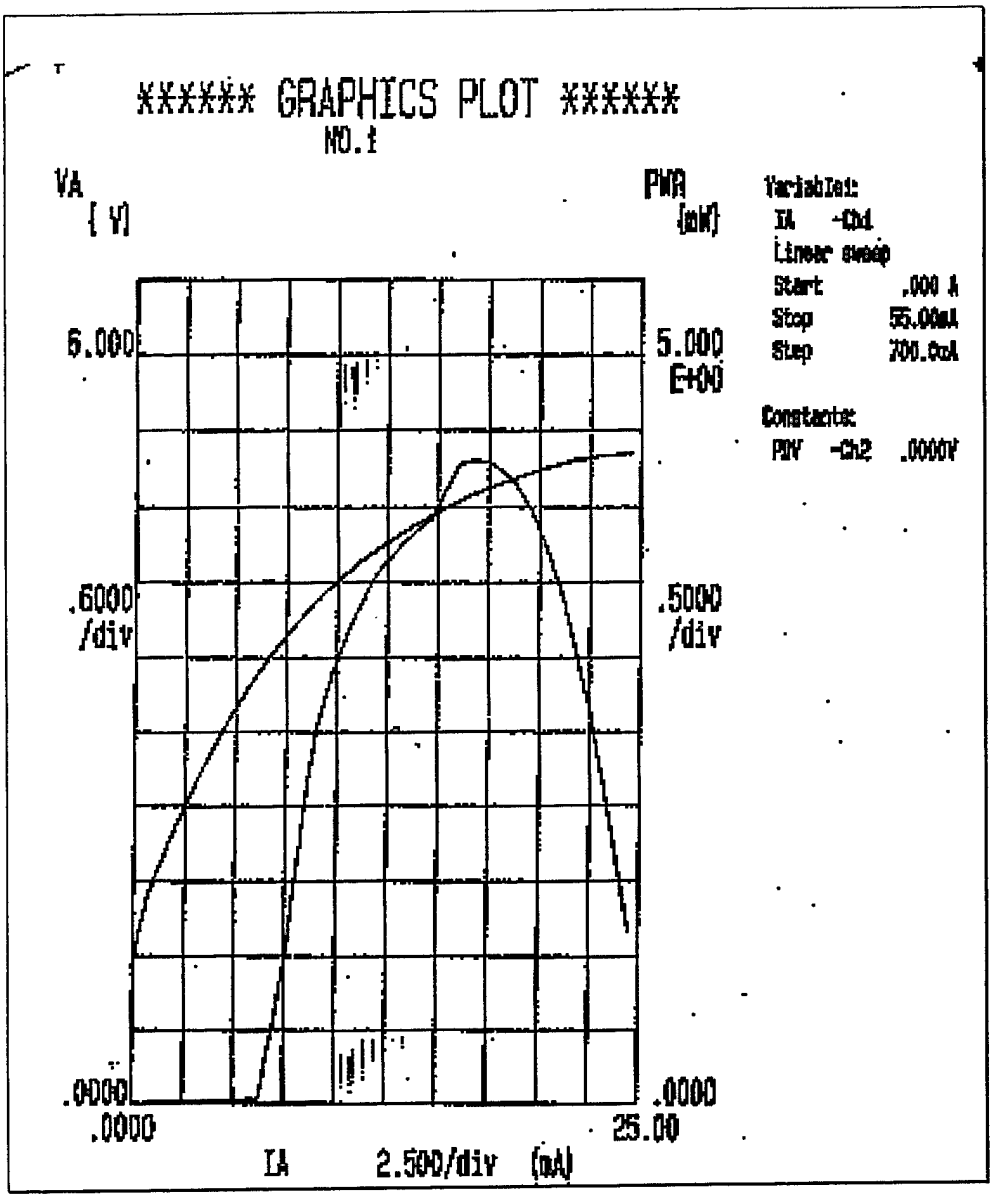


Figure 6 Phase 2 VCSEL Performance

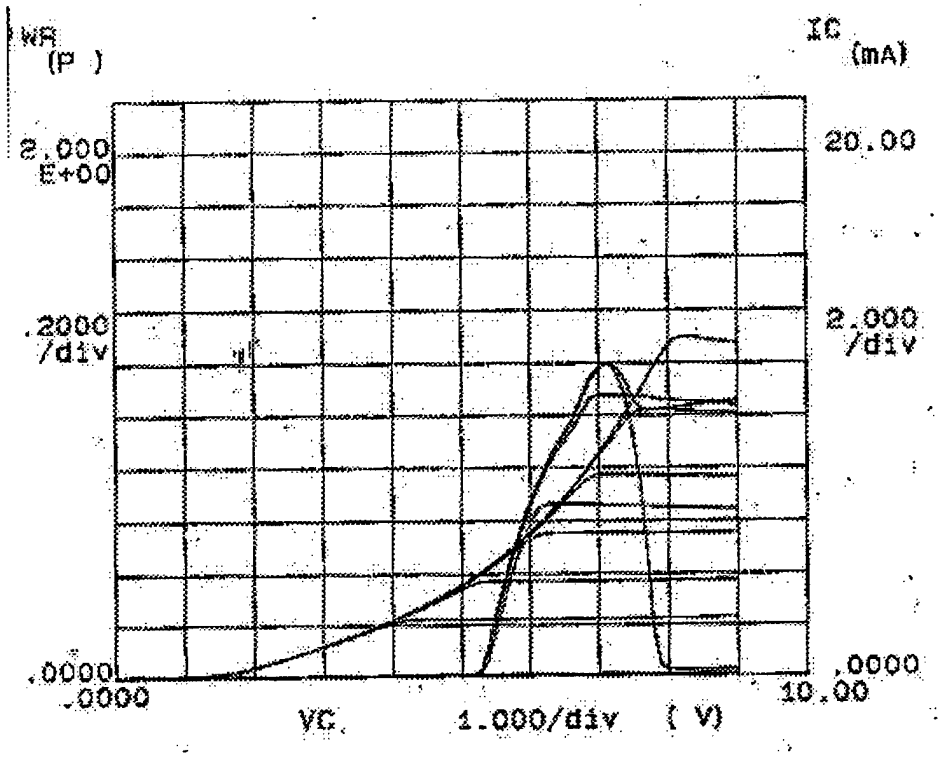


Figure 7 Phase 2 HBT Characteristics and VCSEL Output

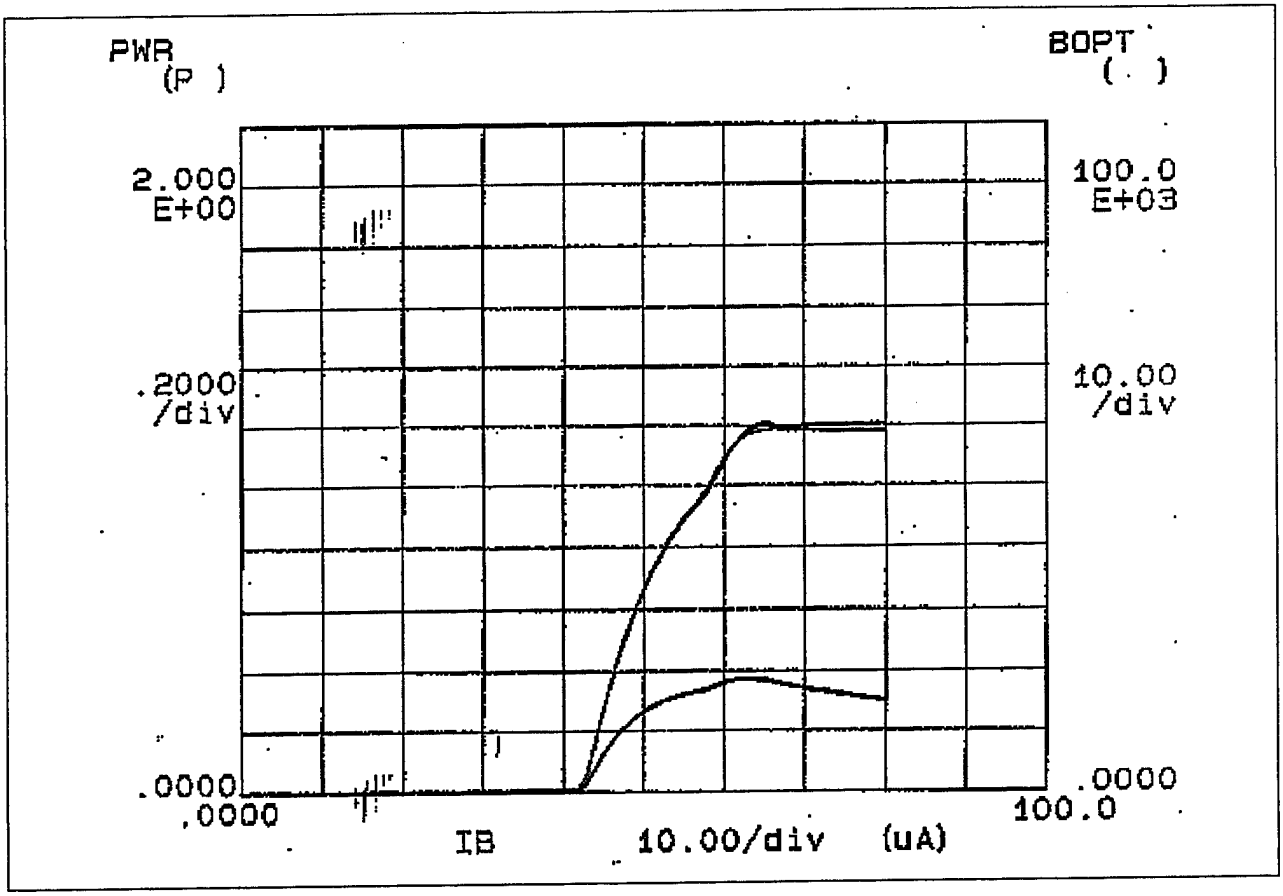


Figure 8 Phase 2 HBT base current vs VCSEL Optical Output.

In addition to the work on the HBT-VCSEL we examined different approaches for power monitoring of a VCSEL. For edge-emitting lasers the laser and monitor are discrete elements. The monitor, a photodiode, is positioned to collect the emission from the back facet of the edge emitter. The photo-generated current in the monitor is collected by the drive circuitry and used to maintain a stable output power from the laser. The main challenge with monitoring the output power from a VCSEL is that the back facet is not accessible from the top surface emitting lasers. Consequently we had to develop a new approach for monitoring VCSELs.

For most applications, the "back-emitted" beam goes into the opaque substrate, and the "useful" beam emits out the top. For efficient operation, VCSELs are designed to emit nearly all the light out the top. Because the bottom-emitted beam is weak and difficult to access, a monitor which samples a portion of the top-emitted beam is desired. In Figure 9 we illustrate two possible approaches for sampling a portion of the top emitted laser beam. In the first approach we build upon the work conducted in the first portion of this program, namely on the integration of a HBT and VCSEL. Here we replace the HBT with a *pin* photodiode. Since the monolithic VCSEL/photodiode is fabricated entirely by wafer-scale processing, its manufacturing cost should be minimized.

The wafer-scale integration should also eliminate a problem associated with the discrete element method used for edge emitting lasers. Although the response of the photodiodes is typically highly reproducible from photodiode to photodiode, the placement of the laser and the placement of the photodiode are not reproducible from component to component. The variation in placement of the discrete elements leads to a variation in the photodiode current-to-laser power correction factor from component to component (this correction factor may vary as much as 30 percent from one component to another). The monolithic

integration of the photodiode to the laser should eliminate the variation in the correction factor and thus lead to a more reproducible, lower cost element.

We also considered an alternative to the monolithic integration of the photodiode to the laser. The bottom of Figure 9 shows hybrid integration of a VCSEL with a monitor and integrated automatic power control circuit on separate substrates. The two substrates must be aligned and bonded, for example by passive-self-aligning solder-bump bonding. Although this represents a significant additional packaging step, the second substrate can straightforwardly exhibit a great deal of functionality. As shown, the substrate comprises sapphire and is outfitted with additional circuitry to perform the APC. Although not shown, it is also possible to fabricate micro-lenses on the opposite side of the sapphire substrate.

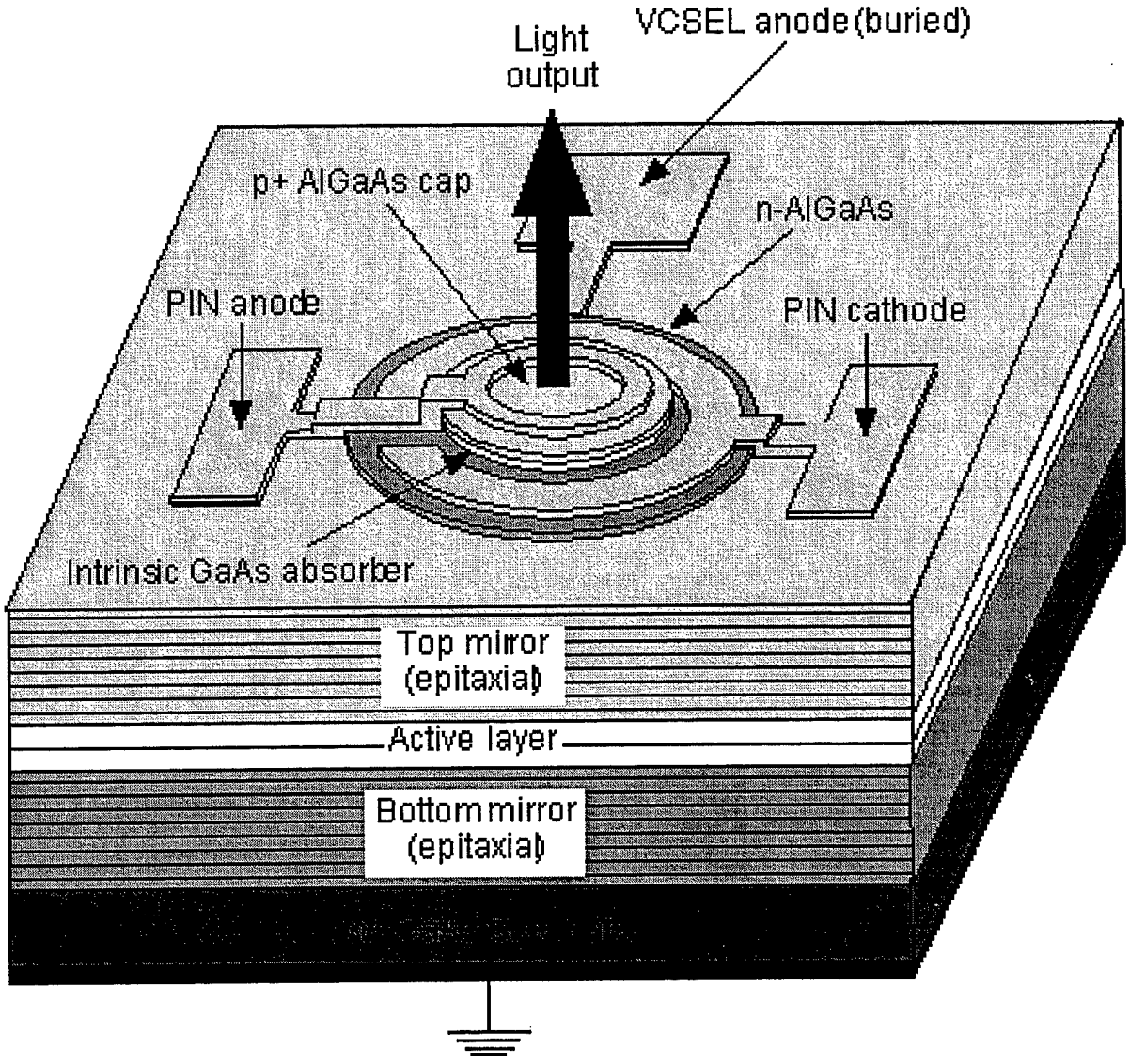


Figure 9 Monolithic Integration of photodiode monitor and VCSEL

The monolithic approach was attempted first. In order to limit the light absorbed by the PIN contacts (non-useful) and maximize the light absorbed by the photodetector (useful) two refinements were made to the design. Using VCSEL modeling software the metal contacts were placed at the nodes of the lasing standing wave pattern while the active area of the photodetector was placed at an anti-node. In this way the contacts produced minimal absorption while the efficiency of the photodetector was maximized.

Two process issues were identified with regard to the potential shorting of the PIN contacts. Due to the extremely thin layers used in the photodetector, there existed the possibility of alloying through the contact layers. In addition, in order to maximize the performance of the PIN, the contacts must be placed as close as possible, further increasing the chances of shorts due to poor alignment. These issues were resolved through careful mask layout and processing of the wafers.

Successful operation of a PIN-VCSEL device was demonstrated. Figure 10 shows the light-current curve for the VCSEL and the photocurrent-VCSEL bias curve for the detector. The photocurrent from the detector reproduces all the major features of the VCSEL L-I curve. In addition the maximum measured photocurrent, 100 μA, far exceeded the design goal of 10 μA. However, some issues remained to be resolved. First, a significant photodiode leakage current was found. Second, this particular design produced too much photocurrent. Third, the practical issue of proper bias conditions for common-cathode arrays remained unresolved.

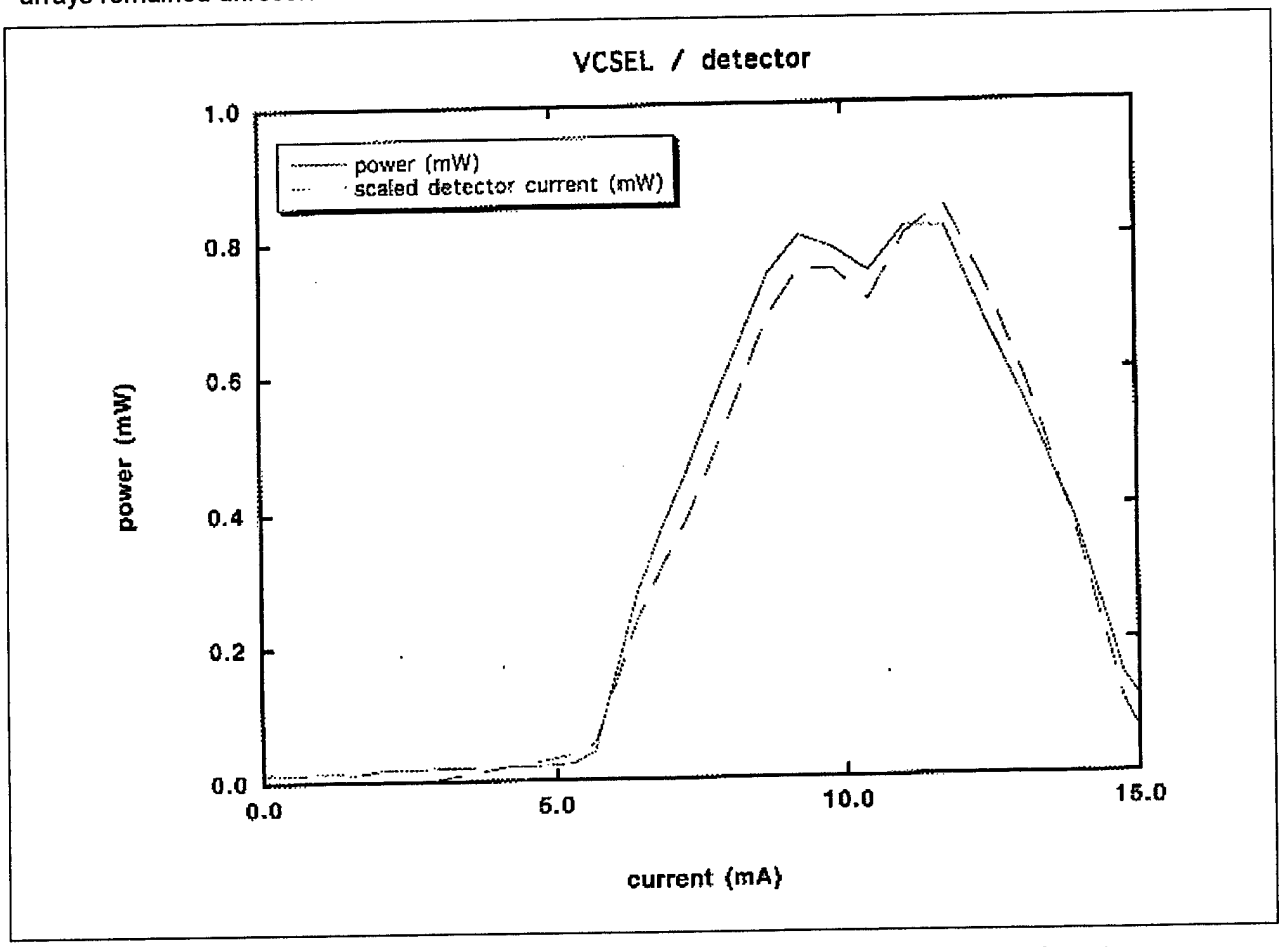


Figure 10 VCSEL L-I curve and photocurrent-VCSEL bias curve for the detector.

Significant progress was made in resolving the last two issues. Reducing the thickness of the PIN intrinsic region both reduced the amount of photocurrent and increased the output of the VCSEL. For the common-cathode VCSEL array it was found that biasing the cathode of the PIN at a fixed voltage above

the anode of the VCSEL worked well. In this configuration, which is given in Figure 11, the anode of the VCSEL and the anode of the PIN are common. From a circuit standpoint, however, it would be desirable to configure the PINs in a common-cathode configuration, while maintaining a fixed voltage across the device. Device designs which would allow this are subjects for future research.

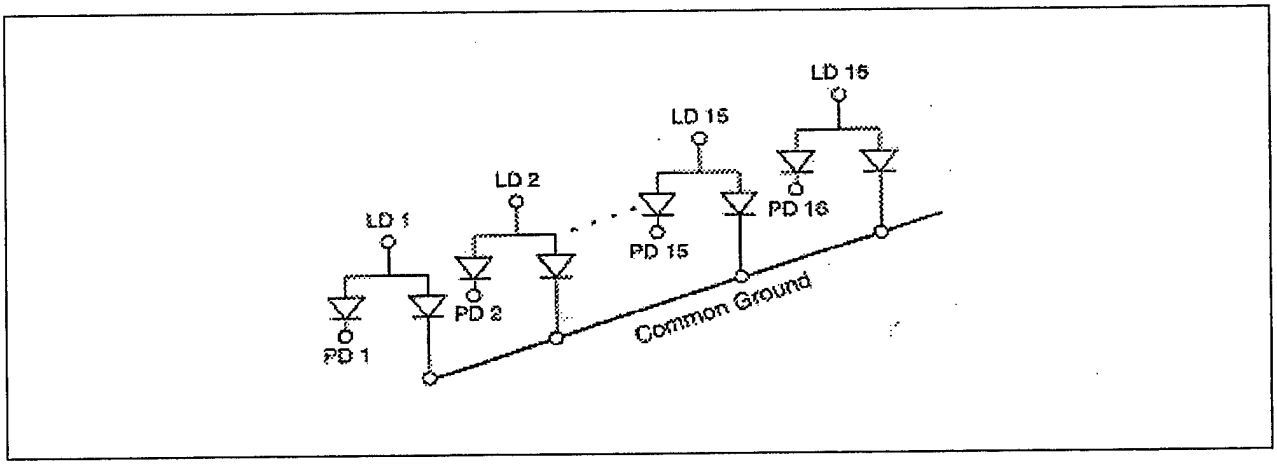


Figure 11 Common cathode VCSEL array configuration.

In summary, the basic building block of automatic power control, the integrated power monitor, was designed, fabricated and successfully demonstrated during the second phase of this contract.

5.3 Phase 3

5.3.1 Introduction

Phase 3 focused on integrating PIN detector diodes and VCSELs in a side-by-side arrangement. This contract supported part of the work described in the rest of this section. The work also received support from the NAVY Small Business Innovation Research Program Contract N62269-93-C-0553. The description following is adapted from a conference paper submitted to the 1997 LEOS Summer Topical Meetings in Montreal, Canada.

This work was proposed because of the recognition that high speed, dense arrays of vertical cavity lasers and detectors are at the core of many optically-interconnected computers and optical processors. In both applications, desired VCSEL properties include low threshold current and voltage, high single-mode power, high contrast and excellent array uniformity; desired detector characteristics include high speed and responsivity. In the conference paper, we presented a general purpose optical interconnect device for optical computing applications. The device is comprised of a monolithically integrated vertical-cavity laser (VCSEL) and PIN photodiode array. As an optical interconnect element, it functions as a bi-directional electro-optic interface; as an optical processing element or smart pixel, it can be coupled with external circuitry to provide arbitrary transfer functions. Device parameters and layout have been optimized for excellent overall performance and easy system insertion.

5.3.2 Device Structure and Layout

The integrated VCSEL-PIN structure is depicted in Figure 12. The growth of the VCSEL/PIN wafer is accomplished by first growing the VCSEL structure and a stop etch layer followed by the photodiode in n-i-p configuration. The device fabrication includes a mesa etch to isolate the PIN from the VCSEL. Top contacts are provided for the PIN anode and cathode, while the VCSEL is contacted from opposite sides of the wafer.

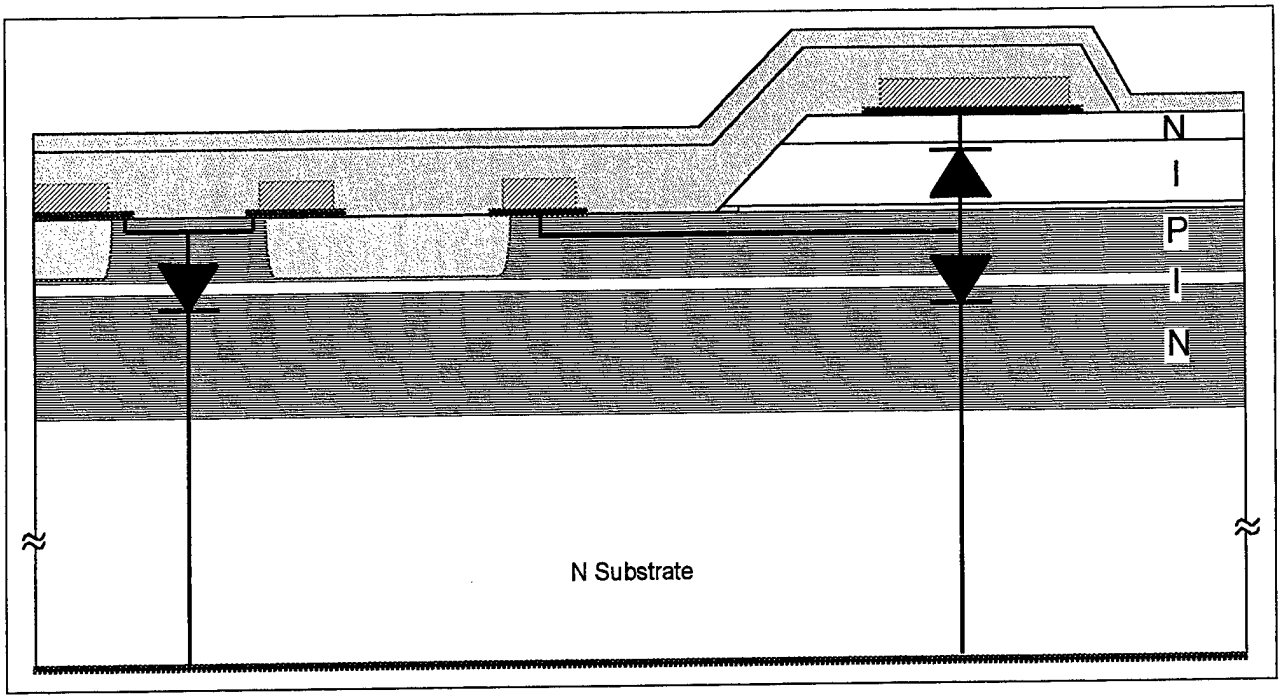


Figure 12 Layer structure of the integrated VCSEL-PIN.

The devices are laid out in a 2x16 array on a 250 µm (horizontal) and 750 µm (vertical) pitch with VCSELs on the top row and PINs on the bottom row, as illustrated in Figure 13. The VCSEL wavelength is 850 nm with a maximum aperture dimension of 8 µm. The PINs have an aperture of 140 µm.

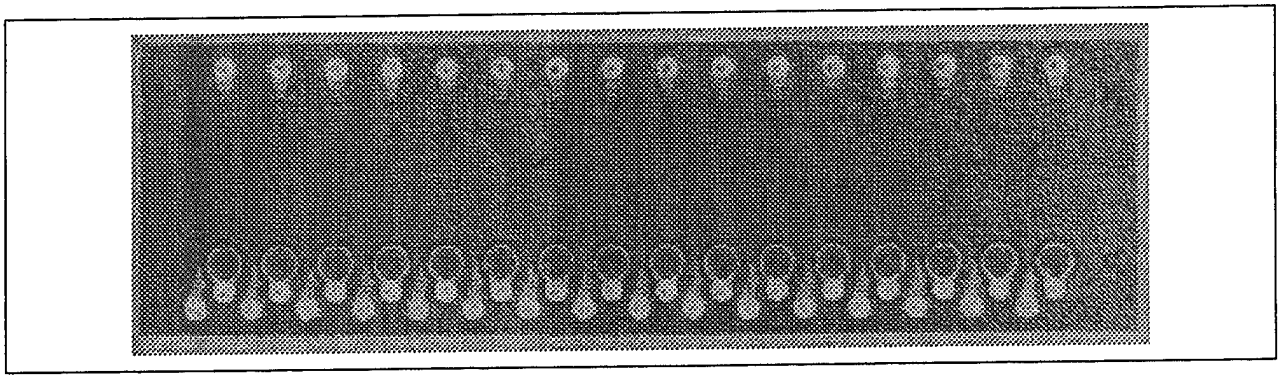


Figure 13 Layout of the integrated 2x16 VCSEL-PIN array

5.3.3 VCSEL and PIN Characteristics

VCSEL thresholds are typically 2.5 mA and 2.2 V. The lasers achieve maximum single-mode output powers of over 1 mW. The threshold is temperature-insensitive over a broad range of temperatures. Figure 14 illustrates the L-I response over the 0 to 90°C temperature range. No appreciable increase in threshold occurs from 0 to 60°C.

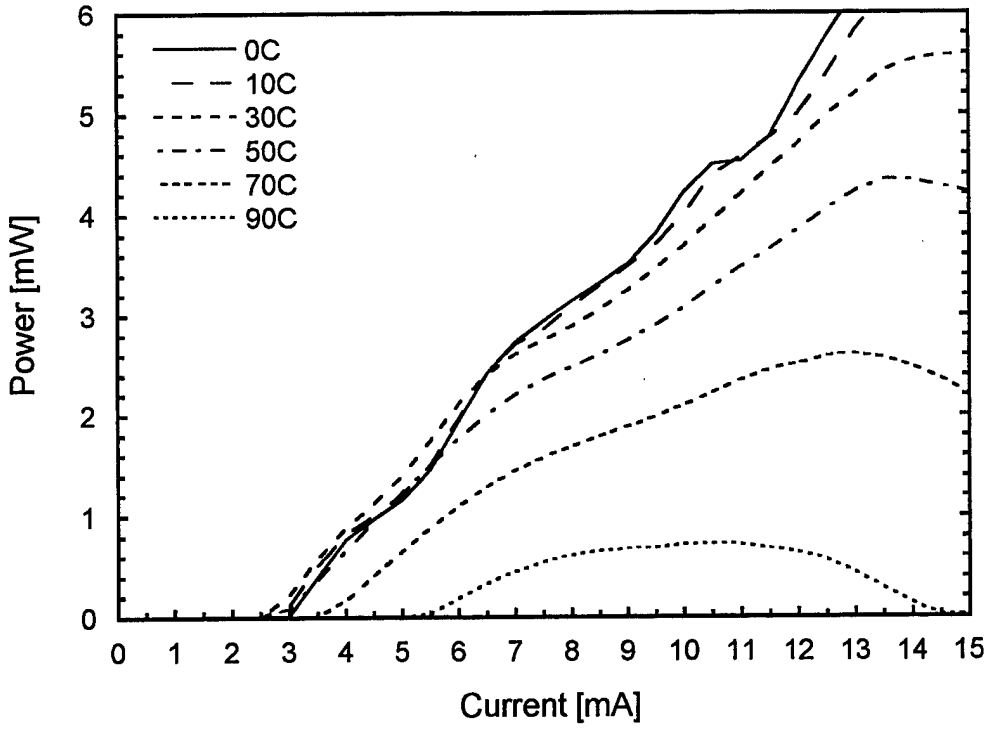


Figure 14 Temperature performance of an 8 μm diameter VCSEL laser.

Optical interconnects require excellent power uniformity over the laser array. Figure 15 shows good VCSEL uniformity across a sixteen element array. In polarization-based optical processors, polarization control and uniformity are important device requirements. Although single-mode lasers are naturally polarized with a large rejection ratio, the polarization direction can vary from laser to laser. We have demonstrated polarization control through the use of oval-shaped apertures. Figure 16 shows the polarized L-I characteristics of an oval aperture VCSEL. An average rejection ratio of 25 dB is achieved throughout the single-mode regime.

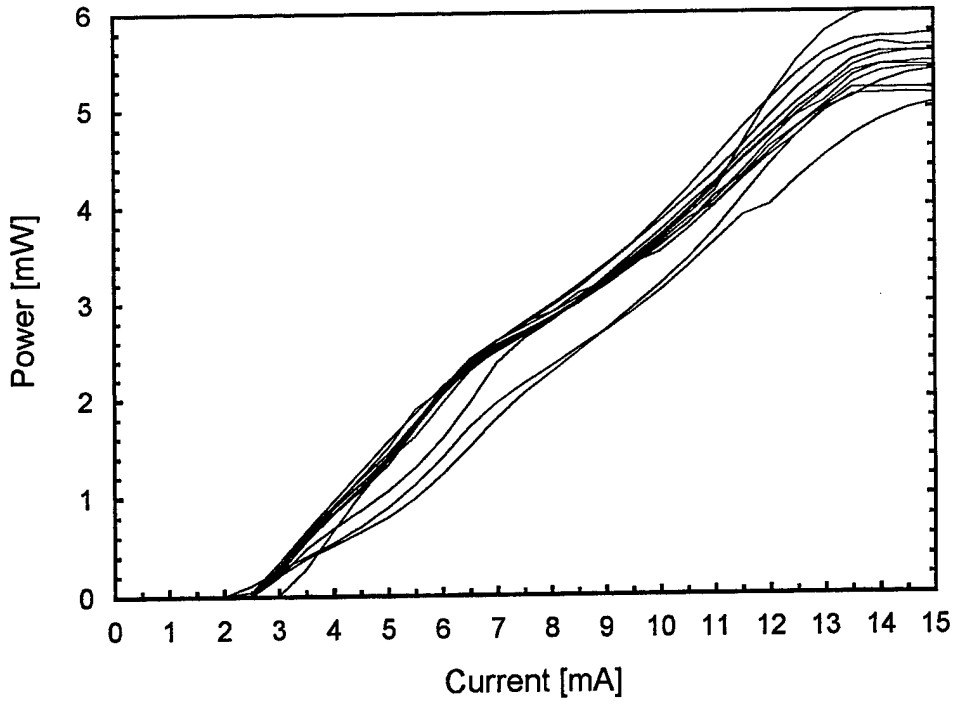


Figure 15 Uniformity of 1x16 array of 8 µm diameter VCLs.

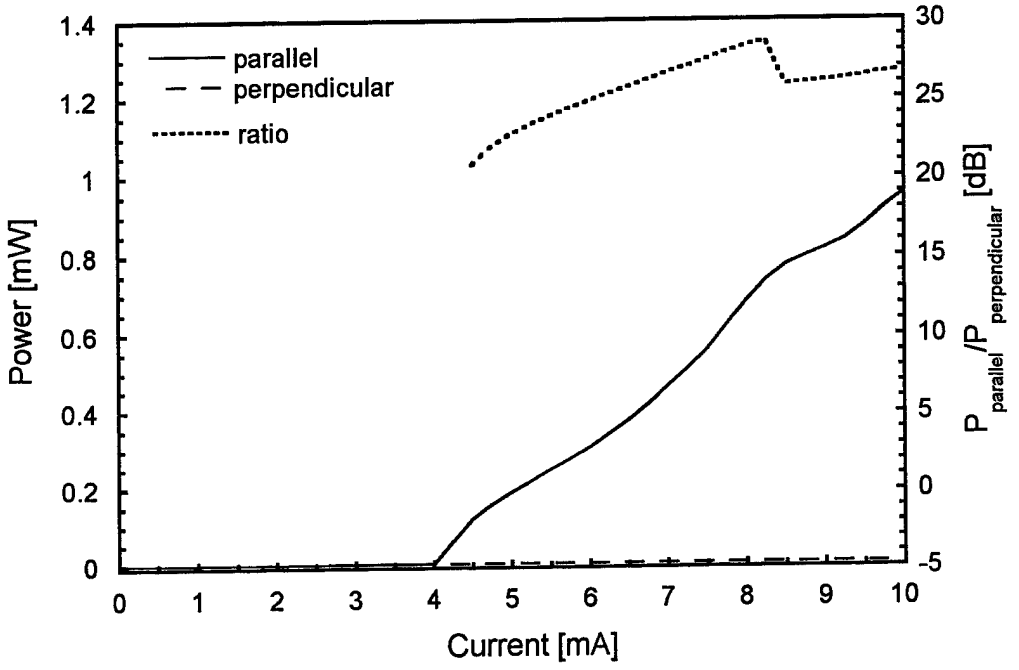


Figure 16 Polarization of an oval-shaped aperture VCSEL.

For optical data links, the lasers have been characterized for relative intensity noise (RIN). Figure 17 demonstrates that VCLs maintain a RIN below -120 dB/Hz for all currents above threshold.

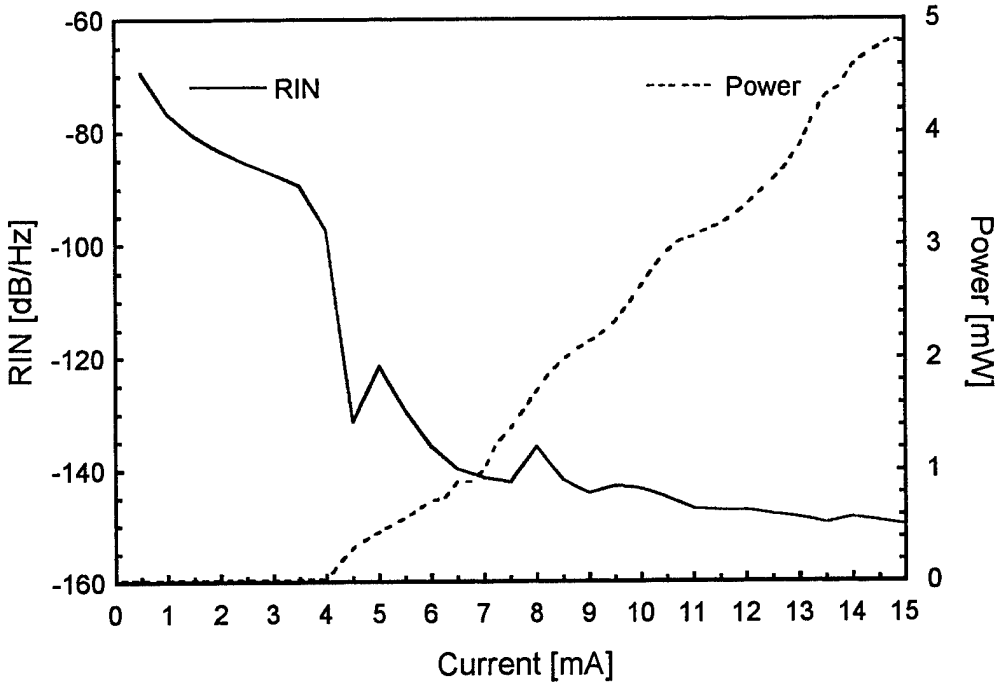


Figure 17 RIN and power versus current for a single-mode 8 μm diameter VCSEL.

The PIN photodiodes exhibit a responsivity of 0.535 A/W, while maintaining a low dark current of 10 nA at a bias voltage of -5 V. The -3 dB bandwidth of the 140-μm diameter detectors was measured to be 2.3 GHz. The frequency response is shown in Figure 18.

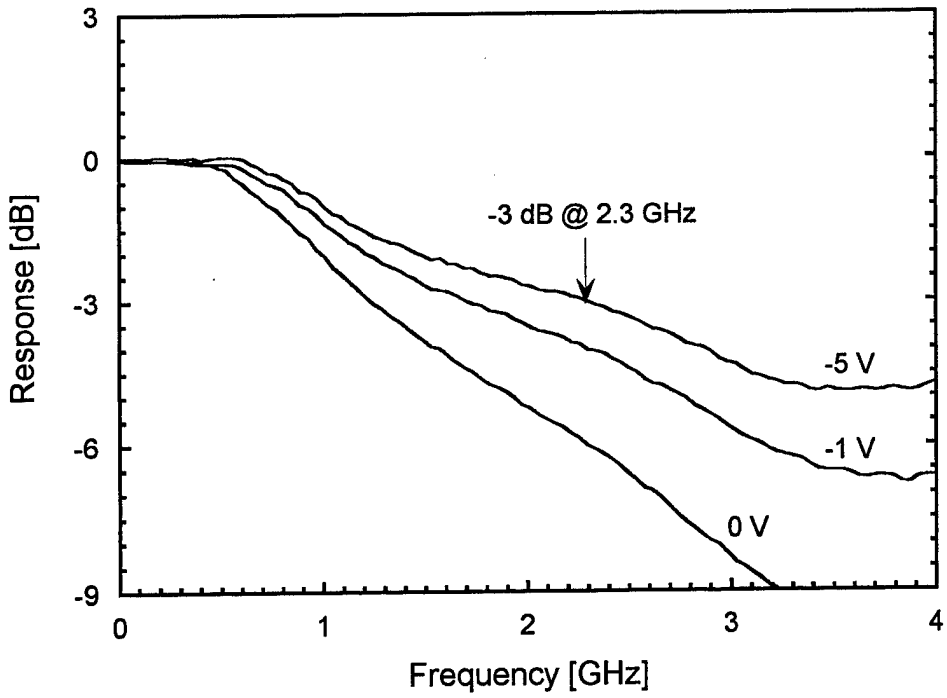


Figure 18 140-μm PIN photodetector frequency response for various levels of reverse bias.

6 Conclusions and Recommendations for Future Work

In phase 1 we designed, fabricated and characterized a basic building block of optoelectronic integrated cuircuits, the integrated HBT-VCSEL. The transistor-driven operation of a VCSEL was successfully demonstrated with a threshold base current of 48 μA. The key technologies for realization of this device were:

- the Au-post implant mask,
- the graded p-mirror interfaces,
- the GaAs isolation layer, and
- the airbridge interconnect.

Future work should focus on improving the individual device characteristics of the HBT and the VCSEL and developing optical input for the base current thus demonstrating an HBPT device.

In phase 2 we improved the performance of the HBT-VCSEL device. In addition to lowering the resistance and threshold of the VCSEL, the gain characteristics of the HBT were improved. The threshold base current was lowered to 43 μA. Future work should include the development of an integrated FET-VCSEL and improvement of the isolation-layer characteristics.

Also in phase two we considered various designs for integrated optical power monitoring and control for the VCSEL. We selected the simplest design for implementation, a PIN integrated onto the output mirror of a VCSEL. This design was grown, fabricated and characterized. Successful operation was demonstrated. The key design technologies were:

- placing the contacts at the node of the electric field standing wave to minimized absorption, and
- placing the absorption region of the PIN at an antinode in order to increase efficiency.

The major processing challenge was to avoid shorting of the contacts due to thin contact layers and small contact geometries. Both issues were avoided through careful mask layout and processing. Future work in this area has been obviated by the great improvements in VCSEL performance and array uniformity over the last few years.

In phase 3 we fabricated and characterized an integrated 2x16 VCSEL/PIN array. The device was designed to perform as a high performance, multi-functional electrooptic building block for optical computing applications. VCSEL arrays exhibit over 1 mW single-mode power with good power uniformity at low thresholds, while PIN arrays concurrently achieve 0.535 A/W responsivity. Future work should focus on improving array uniformity for both PINs and VCSELs and robust and automated alignment and packaging technologies.

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8 Program Timeline – Summary of Accomplishments

Date	Summary
8/18/92	Program begins.
9/25/92	Device design completed for transistors FETs and HBTs and VCLs.
10/31/92	Obtained processing and growth subcontractors, David Sarnoff and EPI. Layout of VCSEL mask.
12/31/92	First VCLs grown, modifications made. Process development under way. PL and reflectometry setup.
1/31/93	Growth problems. Evaluated Lockheed material (achieved optically pumped lasing). Process modifications for implant.
2/28/93	Low voltage VCSEL achieved. Test plans completed for VCSEL, HBT, and FET.
3/31/93	Better implant mask developed. High-Al-content AlGaAs proposed as isolation layer between HBT and VCSEL. EPI growing test structures. Test plan submitted.
4/30/93	Implant matrix complete. VCLs successfully processed. Incomplete dielectric removal caused high voltages and series resistance. Lockheed material better than EPI.
5/31/93	PRI buys a PlasmaTherm deposition system. Two isolation layers being explored, AlGaAs and GaAs, both with etch stop layers. EPI material improving. PRI considering pulling plug on some subcontractors.
6/30/93	Insulating layer growths at Lockheed. Performed packaging pull test. PRI moves to Longmont.
7/31/93	P-mirror resistance too high. Modified VCSEL design to grow on an MBE reactor.
8/31/93	Investigated p-contact as source of high resistance. Result was negative. Conclusion: doping in the p-mirror is too low. Ruled-out low temp AlGaAs for isolation layer. Design and process modifications complete. Mask modifications initiated. Fabrication facility still under construction. MBE reactor on its way.
9/30/93	Proposed expansion of contract objectives to developing optoelectronic interconnects. Fabrication facility still under construction. MBE reactor on its way. SEM ordered. Mask modification complete.
10/31/93	MBE arrives. Further development of electroplated implant mask and dielectric mirrors.
11/30/93	MBE calibration starts. Complete processing runs start. VCSEL contact layer modified. Autoprobe system purchased.
12/31/93	First VCSEL and HBT wafers grown. VCLs showed high series resistance due to abrupt interfaces in the p-mirror. Switch to graded interfaces. Wavelength uniformity measured to be $\leq$ 3%.
1/31/94	First LIV plots shown.
2/28/94	First HBT wafers completed and measured. Good performance. Unrepeatable measurements due to tester problem.
3/31/94	Improved output power and LIVs. Fixed testing problem on HBTs. MBE vents. Added thermal chuck to autoprober for temperature characterization.
4/30/94	Measured thermal resistivity: ~2600 K/W, which is 10 to 50X edge emitter value. T_0 = 140 °K. First HBT plot. Base-emitter junction needs improvement by reducing base thickness. PRI considering purchase of Bandgap.
5/31/94	Series of HBT measurements submitted.
6/30/94	Reiteration of HBT/VCSEL integrated structural design. Outline of process. Etch development complete. Air bridge technology identified as important to develop. SEMs of HBTs on VCSEL substrates shown.
7/31/94	Air bridge development continues. Additional HBT SEMs shown. PRI buys Bandgap.
8/31/94	Two wafers completed. Additional SEMs shown.
9/31/94	HBT large-signal gain 350. VCSEL Vth = 2.7 V, Ith = 19 mA. Investigating cause of high Ith. HBT-VCSEL base current to reach threshold, Ibth = 48 μA. Ib(1 mW) = 55 μA. Effective efficiency = 150 W/A! HBT-VCSEL leakage path found, breakdown @ 4.5 V. Curves included.

Date	Summary
10/31/94	Modified isolation layer. New growths completed. New processing initiated.
11/30/94	HBTs measured. Gain = 400, Differential gain = 530. Processing continued. Redefined goals for third year of contract: Demonstrate improved HBT-VCSEL. Continue to search for applications of this technology. Focus on automatic power control (APC) applications, especially those relating to laser printing, data communications, and sensor applications. Develop automatic power control. Demonstrate power monitoring in VCSEL-based device.
12/31/94	HBT-VCSEL improvements in process. Two approaches to APC are outlined: Growing PIN photodiode on top of VCSEL (light emits through photodiode). Hybrid solution in which the diodes are fabricated on a separate sapphire substrate and flip chip aligned to the VCSEL (light emits through photodiode).
1/31/95	Completed revision on HBT-VCSEL improvements. PIN-VCSEL approach adopted for APC. Refinements of placing contact layers at nodes and PIN active at antinode are added.
2/28/95	HBT-VCSEL improvements measured: Ith = 5 - 7 mA. Vth = 3 - 3.5 V. Pmax = 4 - 5 mW. Ibth = 43 μA. Gp = 20 mW/mA. HBT-VCSEL work completed.
3/31/95	Process issues identified with regard to shorting of the PIN contacts due to 1) thin layers and 2) tight alignment tolerances.
4/30/95	PIN contact process development completed.
5/31/95	Successful demonstration of PIN-VCSEL operation. No plots were given. Remaining issues include 1) photodiode leakage, 2) too much photocurrent and 3) proper bias conditions to monitor a common-cathode array.
6/30/95	Demonstrated successful power monitoring via floating PIN cathode biasing scheme.
1/31/96	Vixel proposes redirection of program goals toward transmitter-receiver VCSEL-PIN arrays.
4/30/96	Rome approves redirection of program goals.
8/16/96	Final Program Review takes place in Broomfield.
8/11/97	VCSEL/PIN Invited Paper is presented at LEOS Summer Topicals
7/98	Final Report is submitted.

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